AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A semiconductor device formed on a substrate, comprising:

an interconnection line formed on said substrate and provided to structure a prescribed circuit; and

a fuse incorporated into said interconnection line,

said fuse and a connection portion of said interconnection line electrically connected to the fuse being formed of different metals, wherein:

an oxidation speed of the metal forming said fuse is faster than an oxidation speed of the metal forming the connection portion of said interconnection line;

said fuse is formed of a copper metal;

the connection portion of said interconnection line is formed of an aluminum metal; and

said copper fuse is flat so that focusing can be easily obtained.

2. (Cancelled).

3. (Cancelled)

4. (Currently Amended) The semiconductor device according to claim 1 ~~3~~, wherein said fuse is formed of the copper metal formed in a damascene process and planarized by a CMP (Chemical Mechanical Polishing) process.

5. (Previously Presented) A semiconductor device formed on a substrate, comprising:

an interconnection line formed on said substrate and provided to structure a prescribed circuit; and

a fuse incorporated into said interconnection line,

said fuse and a connection portion of said interconnection line electrically connected to the fuse being formed of different metals, wherein

said interconnection line is formed as a multilayer interconnection line,

said fuse is provided at a same layer as one layer of the multilayer interconnection line, and

an antireflection layer is provided closer to said substrate than a layer of said fuse is.

6. (Original) The semiconductor device according to claim 5, wherein

said antireflection layer includes a first antireflection layer extending in a direction of a length of said fuse, and a second antireflection layer extending in a direction traversing the first antireflection layer.

7. (Previously Presented) A semiconductor device formed on a substrate, comprising:

an interconnection line formed on said substrate and provided to structure a prescribed circuit; and

a fuse incorporated into said interconnection line,

said fuse and a connection portion of said interconnection line electrically connected to the fuse being formed of different metals, wherein

said interconnection line is formed as a multilayer interconnection line,

said fuse is provided at a same layer as one layer of the multilayer interconnection line, and

a reflection layer is provided closer to said substrate than a layer of said fuse is.

8. (Original) The semiconductor device according to claim 7, wherein said reflection layer includes a dummy metal line provided between said fuses in a planar view and a transparent resin film covering the dummy metal line, said transparent resin film forming a recessed and protruded surface having a portion overlying the dummy metal line and projecting closer to said fuse than a portion between the dummy metal lines.

9. (Currently Amended) The semiconductor device according to claim 1, wherein said fuse is formed from at least two portions different in width.[[.]]

10. (Previously Presented) The semiconductor device according to claim 1, wherein said fuse has a width gradually reduced from an end toward an intermediate portion of said fuse.

11. (Original) The semiconductor device according to claim 10, wherein said fuse has at least three different widths from the end toward the intermediate portion.